REMARKS

Claims 2-5, 7-9, 11-19 and 22-49 are pending in the above-referenced patent application. In this amendment, claims 2-5, 8-9, 11-14, 17-19, 22-27, 32 and 44 have been amended, claims 10 and 20-21 have been cancelled, and no claims have been added. It is noted that the claim amendments and cancellations were not made in light of cited references, but, rather, were made to more clearly delineate intended subject matter. Furthermore, it is believed that the amendments do not narrow claim scope. Rather, in some circumstances, the claims may even be broadened. Therefore, no prosecution history estoppel should result from these claim amendments and cancellations.

Claim Rejections – 35 U.S.C §102(e)

In the Final Office Action, dated April 20, 2006, claims 2-3, 5, 7-9, 17-18, 20-24, 44-46 and 49 are rejected under 35 U.S.C 102(e) as being anticipated by Grisamore (U.S. Patent No. 6,535,901, hereinafter "Grisamore"); claims 4, 10-12, 19 , 25-27 and 47-48 are rejected under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang et al. (Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs, Nov. 1999, IEEE Computers and Digital Techniques, pages 309-315, hereinafter "Chang"); claims 13-16 and 28-31 are rejected under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang et al. ("A hierarchical function structuring and partitioning approach for multiple-FPGA implementations, Oct. 1997, IEEE Computer-Aided Design of Integrated Circuits and Systems, pages 1188-1195, hereinafter "Fang"); claims 32, 36-38 and 42-43 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger (U.S. Patent No. 6,411,979, hereinafter "Greenberger"); claims 33-35 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang; claims 39-41 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang, and in further view of Fang. These rejections are respectfully traversed.

Claim Rejection – 102(e)

Grisamore

Assignee respectfully submits that Grisamore does not set forth each and every element of the rejected claims, as amended, and, therefore, contrary to the Examiner's assertion, the claims are not anticipated by Grisamore under 35 U.S.C. 102(e). For example, referring to claim 2, as amended, which recites, in part:

> a summing module generator coupled with a dedicated logic device, wherein the dedicated logic device is coupled with the plurality of inputs, wherein the summing module generator is adapted to structure atomic elements of the dedicated logic device to implement a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers, wherein the summing module is adapted to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern such that input bits of equal significance are partitioned into groups of three to serve as inputs to full-adders, remaining groups of two to serve as inputs to half-adders, and remaining single bits to serve as inputs to single registers, wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, at least a portion of the plurality of inputs adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results.

Failure to Recite "Associated Registers"

Grisamore does not show or describe at least "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers" as recited in claim 2, as amended. Grisamore clearly describes passing partial products to an adder to perform adding functions, and passing and subsequently retrieving carry terms from a memory device [Col. 2:63-3:8.], rather than utilizing an apparatus having associated registers. Assignee is unable to find any description throughout Grisamore of registers implemented in a manner

as recited in the rejected claims. It is respectfully requested that the Examiner cite the portion of Grisamore that describes registers implemented outside a memory device, and implemented as one or more full-adders and associated registers, half-adders and associated registers, and single registers, as recited in the rejected claims.

Further, the cited portion of Grisamore, referenced from the Background section, describe registers implemented in an array multiplier, and does not show or describe registers implemented in "a multi-stage series of Boolean function generators", as claimed in claim 2. Therefore, it is respectfully submitted that Grisamore does not show or describe "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers" as recited in claim 2, and, therefore, Grisamore fails to set forth each and every element of the rejected claims.

Failure to Recite "An Integrated Multi-Input Adder"

Grisamore additionally does not show or describe "an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, at least a portion of the plurality of inputs adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results.", as recited in claim 2, as amended. Grisamore clearly describes utilizing a memory to perform adding functions of accumulator bits. For example, quoting from col 3:28 – col 3:30, "The adder 18, which may be a carry look-ahead adder, receives the first and second preceding resultants 26 and 28 and produces a multiplied accumulated resultant 34." As can be clearly seen from this excerpt, along with Fig. 1, the "adder" of Grisamore performs adding functions to provide an accumulated resultant, and is not "an integrated multi-input adder", as it is not integrated into the "reduction tree module", but, rather, is a separate component utilized to perform adding functions.

It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that this ground is sufficient. Assignee respectfully submits that because Grisamore does not does not set forth each and every element of the rejected claims, claim 2 is in a condition for allowance. Additionally, claims 3, 5, 7-9, 17-18, 22-24, 44-46 and 49 are in a condition for allowance for the same and/or similar reasons as presented with reference to claim 2, as amended. It is respectfully requested that the Examiner withdraw his rejections of these claims also. It is noted that claims 20-21 have been cancelled, and, therefore, this rejection of claims 20-21 is moot.

Claim Rejections – 35 U.S.C §103(a)

The Examiner has rejected claims 4, 10-12, 19 , 25-27 and 47-48 under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang et al.; rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang et al.; rejected claims 32, 36-38 and 42-43 under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger; rejected claims 33-35 under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang; and rejected claims 39-41 under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang, and in further view of Fang. These rejections are respectfully traversed.

Grisamore v Chang

2. Failure to teach all limitations

It is respectfully submitted that claims 4, 11-12, 19, 25-27 and 47-48 are not rendered obvious by Grisamore, whether viewed alone or in combination with Chang. For example, any combination of Grisamore and Chang would still not teach or suggest all the claim limitations. However, Assignee does not by this argument accept that the combination is proper; rather, while Assignee asserts that the combination is improper, Assignee further asserts that even if the combination were proper, the combination would still fail to provide all the elements of the rejected claims.

Assignee begins with claim 4, rejected under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang. The Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose the Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose[s] in Figure 1(a) Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions." However, even if the successful combination of Grisamore and Chang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of claim 4. As just an example, Chang is directed generally toward LUT based FPGAs, and does not show or describe "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers, wherein the summing module is adapted to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern such that input bits of equal significance are partitioned into groups of three to serve as inputs to full-adders, remaining groups of two to serve as inputs to half-adders, and remaining single bits to serve as inputs to single registers, wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, at least a portion of the plurality of inputs adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results." Additionally, as noted above, Grisamore does not cure these deficiencies. Therefore, any resultant combination of Grisamore and Chang would not produce the elements of claim 4.

It is respectfully submitted, therefore, that at least one element of claim 4 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of claim 4. Additionally, claims 11-12, 19, 25-27 and 47-48 distinguish from the cited art for at least the same

reasons. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims. It is noted that claim 10 has been cancelled, and, therefore, this rejection of claim 10 is moot.

Grisamore v Chang v Fang

The Examiner has rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang. This rejection by the Examiner is also respectfully traversed. The Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose in Figures 1, 4-5, and 7 a controller or a logic module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically ... structures the atomic elements of the dedicated logic device." However, even if the successful combination of Grisamore, Chang and Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims. Fang is directed toward structuring and partitioning of FPGA implementations. The cited passage recites hierarchical structuring of an FPGA implementation, and does not provide the deficiencies of Grisamore, noted above. For example, neither Chang nor Fang recite and does not show or describe "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers, wherein the summing module is adapted to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern such that input bits of equal significance are partitioned into groups of three to serve as inputs to full-adders, remaining groups of two to serve as inputs to half-adders, and remaining single bits to serve as inputs to single registers, wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder includes a plurality of inputs, at least a portion of the plurality of inputs adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and

associated registers, and single registers of the summing module and further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results.", as recited in claim 2, from which claim 13 depends. Additionally, as noted above, Grisamore does not cure these deficiencies. Therefore, any resultant combination of Grisamore and Chang would not produce the elements of claims 13-16 and 28-31.

It is respectfully submitted, therefore, that at least one element of claims 13-16 and 28-31 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of the rejected claims. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Grisamore v Greenburger v Chang

The Examiner has rejected claims 32, 36-38, and 42-43 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, claims 33-35 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, further in view of Chang, and claims 39-41 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, in further view of Chang, in further view of Fang. Beginning with claim 32, the Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not implicitly disclose two paths one for a real component branch, inverting certain partial produces and passing the inverted and non-inverted partial products and one for an imaginary component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously." It is respectfully submitted that even if the successful combination of Grisamore with Greenburger, and/or Chang and/or Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims.

Greenburger is directed toward a complex number multiplier circuit, and does not provide the deficiencies of Grisamore and/or Chang and/or Fang, noted above. For example, neither Chang, Fang nor Greenburger teach or suggest at least "simultaneously passing the partial products from the two or more input terms to a multi-stage series of Boolean function generators that implements one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products; determining the structure of the Boolean function generators based, at least in part, on one or more attributes of the input terms; receiving in both branches accumulator bits over a feedback path, wherein the accumulator bits are respectively provided to an integrated multi-input adder; and adding the intermediate summation results with the accumulator bits for each branch to produce a final real-component sum and a final imaginary-component sum.", as recited in claim 32, as amended. Additionally, as noted above, Grisamore does not cure these deficiencies. Therefore, any resultant combination of Grisamore and

Chang, Fang nor Greenburger would not produce the elements of claim 32, as amended. Claims 33-43 depend from and include all limitations of claim 32, and distinguish from the cited art at least on the same basis as claim 32.

It is respectfully submitted, therefore, that at least one element of claims 32-43 is absent from the cited art, and any alleged combination would still not teach or suggest all of the elements of the rejected claims. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Assignee respectfully submits that, for at least the reasons presented above, the pending claims are not rendered obvious in light of cited references, and, therefore, the rejected claims are in a condition for allowance. It is noted that many other bases for traversing these rejections could be provided, but Assignee believes that this ground is sufficient. It is respectfully requested that the Examiner withdraw this rejections of these claims.

Attorney Docket: 012.P10008

CONCLUSION

In view of the foregoing, it is respectfully submitted that all claims presented are in a condition for allowance, and early allowance of all claims pending in the application is respectfully requested. If the Examiner has any questions, he is invited to contact the undersigned at (503) 439-6500.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3703.

Respectfully submitted,

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